Power Extension of RISC architecture using Clock Gating Technique

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ABSTRACT

Power has become an important aspect in the design of broad-spectrum purpose processors. The unadventurous these mainframes consume too much power as compared with other workstations. This reduction in these computers is done in the manufacture step itself. But this is a complex process. If we can implement the techniques for power reduction in front end process then we can easily design the low power processors without any complication. In this paper we are proposing low power design in front end process. There is lot of techniques to reduce the power. Low control feasting helps to reduce the heat dissipation, lengthen battery life and increase device reliability. This method is designed using pipelined construction; through this can intensification the speed of the process. In this we are using 5-stage pipelining. Concluded the strategy progression we are including various low power enactments in architectural level also. The main power dropping method that has been explored in this planning is clock gating. Clock Gating is a well-known technique to reduce the power consumption in this proposed Application Explicit Processor.

KEYWORDS: *Low power, RISC Processor, Clock gating, Pipelining.*

1. INTRODUCTION

The Interrupt Controller is a machine usually found in computer system which contract with interrupts make by the peripherals and the processors handle the interrupt priority, and legislature the implementation to a computer. The general purpose mainframes provide one or more interrupt request pins that allows external devices to request the service provide by CPU. Think a case in which processor can handle a big number of interrupts which are come from outside plans. The design requires a separate interrupt regulator which is interfaced to the workspace. More over the processor needs some extra- interfacing Circuits which reductions the enactment and proliferation the power consumption of the overall system. The proposed construction combines the interject regulator and RIS central process unit employs an adaptive clock gating to reduce the overall power devouring. Power is the one of the enterprise constraint, which is not only functional to portable computers and mobile communication devices but also for high-end systems. Power excess becomes a bottleneck for future technologies. In the early days designers treat the clock signal should not be restricted or disturbed. But clock signal is a major spring for power intemperance and it is an energetic in nature because clock signal is feed into numerous blocks in the processor. Because all the blocks usage varies within and across a processor, all the blocks not used all the time and gives a chance to reduce the power ingesting of unused blocks. Regulator gating is an efficient technique to reduce the vibrant power intemperance. By ending the clock signal with gated control signal this performance disables the signal to the block when the block is unused. Adaptive technique is one of the techniques used to diminish the dynamic power of the clock. In this method gating allow signal make by the block itself depending upon the practice and this method will decrease the burden on the control unit for make gating signal.

Interrupt handling mechanism provides how interject is handled by processor. There are various techniques to reduce the dynamic clock power dissipation. The supervisortakes two cyclesto process the interrupt. RISI Regulator takes only one cycle for both interrupt request generation and acknowledgement. The following section provides a brief overview of architecture of the RISI SWITCH and explanation about the implementation and hardware consideration. The length of with a brief explanation about each block there in the structural design is given. Finally a few notes on simulation results.

Fig1. RISC Micro Processor

Clock-gating is a technique where the clock indication is prevented from reaching the various modules of the processor. The nonappearance of this signal prevents any register and or flip-flop from varying their value. Hence the input to any combinational logic circuit remains unchanged, and no switching action takes place in those circuits. This architecture consists of the ALU, Port Regulator, Interrupt Switch, Transmitter and the Receiver to apply timer gating technique. These are the major unit in our structural design in terms of number of logic gates. The Control Unit is used for generating the regulator gating signal based on the current instruction. The general purpose mainframes provide one or more interrupt pins that allow external devices to request the services provided by CPU. Consider a case in which workstation can handle a large number of interrupts which are come from peripheral devices. So this paper describes about separate interrupt controller which is interfaced to the processor and also separate phone and receiver modules are interfaced. This interfacing boosts the difficulty of plan and rate of the processor. The following sections will provide a brief overview of architecture of the ASP with timer gating with explanation about the implementation. Then brief depiction about the Control unit, Interfere regulator, Transmitter and Receiver sections of the ASP with regulator gating are given. The first section describes about the overall construction of application specific process. Later the individual modules in the system explained.

2. RISC CLOCK GATING ARCHITECTURE

The power competence is the significant restraint in scheming moveable computers, since lower power consequences in lower in service costs, lower fan noise, and lower cooling requirements. Therefore, inventers of modern portable systems focus on increased system recital while reducing operating power consumption. Increasing the operating frequency, using more powerful, higher density chips achieves increased system performance, but increasing the performance level intensifications power consumption. Power consumption can be controlled during system operation depending upon the dispensation workload. This approach is called active voltage frequency scaling. According to the CPU workload, there are synchronous between the variation of the operating occurrence and supply voltage. For the cases that the workload is less than the minimum supply voltage requirements to drive the CPU, the enable signal of the clock gating performance will activate, during the activation of the enable signal the regulator process unit consumes zero power. Hence the lowest energy

reduction will obtain The clock gating performance categorizes low dispensation requirement periods and reduces operating voltage with clock occurrence (voltage-frequency scaling), resulting in reduced average operating power consumption. According to the CPU workloads, f and V can be reduced to its minimum levels or zero levels based on the software control.

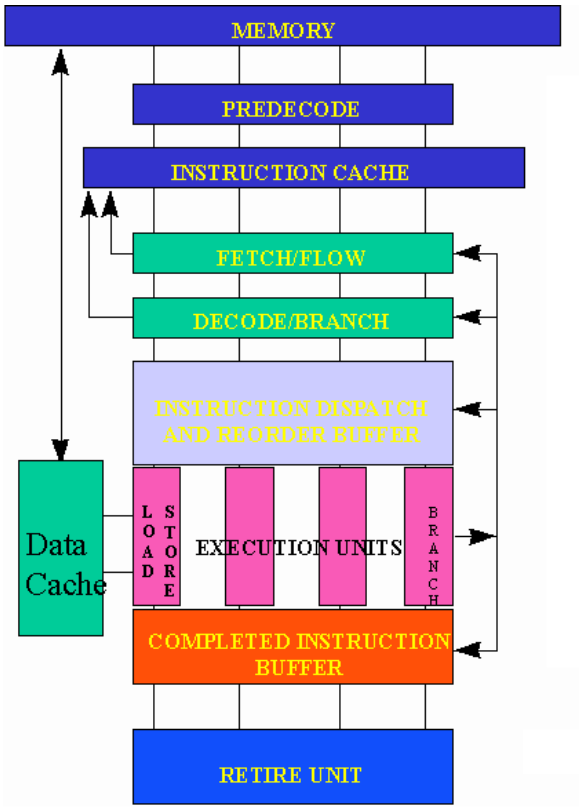

Fig.2. RISC Processor Architecture

2.1 INTERNAL ARCHITECTURE OF RISC CONTROLLER:

The instruction distance end to end of RISC Controller is 16-bit wide. This Regulator has three flags namely carry, zero and interrupt flags. Both zero and carry decorations are affected only during the performance of arithmetic and logical directives and these are also beneficial for determine the flow of execution when branch and jump instructions take place. CPU checks the interrupt flag after achievement of every instruction to know whether interrupt is available or not. ALU is capable of performing the Arithmetic and Logical operations (like And, Or, Xor and Cmpl). There are no particular reason registers in the CPU like collector and there is no main concern among them. An 8-bit address value provided on the bus together with a READ or WRITE strobe signal indicates the accessed point. This address is either supplied in the program as an absolute value or specified indirectly as the contents of any of the eight registers. There are some specific instructions useful for the controlling of interrupt controller present in the RISC CONTROLLER.

2.2 INTERRUPT CONTROLLER:

Present CPUs give one or more interrupt request pins that allows additional devices to ask for the service give by this unit. Intrude controller are used to increase the number of interrupt inputs available to

processor. Interrupt controller composed with three blocks. They are Interfere Register block, Edge interrupt detection unit and Interrupt request generation unit. Interrupts are recognized by interrupt discovery unit throughout the unenthusiastic clock rim of the clock. Whenever disturbs are detected, check for the corresponding intrude input masked or not. Unmasked interrupt input set the corresponding bit in this status register. IRQ generation unit make the interrupt ask for by using the IVR contents. Interrupt ask for arrive at the CPU send an acknowledgement signal. Int_inputs are used to watch the interrupts pending from a variety of peripherals or additional devices. Each interrupt register has a single address and recognized by using Addr input. To write the contents of Data input into the intersect registers require a high valid_wr input. Intr flag input indicates the status of this flag present in the CPU.

Interrupt Detection Unit detects the interrupts coming from peripheral or external devices and actives the logic to produce enable interrupt to controller. It monitors the interrupt inputs composed of interrupt signal coming from exterior devices or peripherals and rises enabled interferes according to arrival signals, Intrude Request Generation component contains the Generation logic of the Interrupts towards the processor. Interrupt needs age group is also configurable as either a pulsate output for an edge responsive ask for or as a level output that is cleared when the get in the way is recognized. Interrupt Registers handles the interject significances, deciding which, interferes are enabled or disabled and managing of interrupt acknowledgements. It holds the following Registers Interrupt Status Register (ISR) point to which interrupts are lively. Every one bits in the ISR are set to zero default. Any bits are set to indicate that the corresponding interrupt is active otherwise no active interrupts are available.

3. CLOCK GATING TECHNIQUE FOR LOW POWER RISC PROCESSOR

We analyze the RISC model first. Any IP core (except combinational circuit) can be modeled as an Determinate State Machine which includes several states: Idle, Ready, Run and so on. Respectively group is a state and each arrow shows a transition from a state to another. The state and the transition will be mapped to the sequential circuit and the combinational circuit correspondingly by separation. When an IP core finishes the work, it enters the idle state and stay there until it assents another solicitation from the system bus. We call each of individuals positions excluding IS working state Hence, all states in an IP core are classified to two classes: IS and WS. When an IP core stays in the IS for particular rotations, it does not need the clock. Consequently, disables the IP clock if the resulting situations are gratified:

1. The present condition of the IP core is IS.

2. There is no entreaty for this IP on the system bus during the modern cycle.

The statuses above also can be articulated as following: If the IP current state is IS and its next state is IS too, the clock is disabled habitually; otherwise, the clock is empowered. We call the route understand the above reason Scout Circuit (SC) which is now a mixture one.

4. FEATURES OF ARCHITECTURE

- Simple Instructions. The designers of CISC constructions estimated extensive use of complex commands because they close the semantic crack. However, in preparation, it chances out that compilers mostly ignore these directives; the fact has been confirmed by several empirical educations. Because of these explanations, RISC designs use simpler directives. Limited fixed length directions (typically 4 bytes) are provided. No orders association load/store with arithmetic.

- Few Statistics types: CISC ISA support a variety of data structures, from simple data types such as integers and characters to multifaceted records structures such as records and assemblies. Observed data suggest that complex facts organizations are used relatively infrequently. RISC supports a few simple documents types efficiently and the complex/missing data types are synthesized from them.

- CISC strategies deliver a large number of this method to support multifaceted facts structures as well as to provide flexibility to admittance. However it leads to problems of variable order performance periods& variable-interval instructions. This causes incompetent directive decoding and scheduling. RISC designs use modest addressing modes and fixed distance orders to facilitate pipelining. Memory -indirect lecture to not deliver.

- Identical General Purpose Catalogues. RISC designs allow any record to be used in any context, simplifying compiler projects.

- Harvard Construction: Reduced order set designs often use a this recollection model, where the instruction stream and the data stream are conceptually detached.

4.1. BENEFITS OF RISC ARCHITECTURE

- RISC purposes use only a few limitations, and these processors cannot use the call directions, and therefore, use a stablemeasurement instruction which is easy to channel.
- This planning has a set of instructions, so high-level etymological compilers can produce more resourceful code.
- It allows independence of using the space on microchips because of its easiness.
- This mainframes used many registers for passing inspirations and holding the local variables.
- Very less number of instructional formats, a few numbers of directives and a few addressing modes are desirable.
- The speed of the process can be exploited and the implementation time can be minimized.

4.2. DRAWBACKS OF RISC ARCHITECTURE

- Mostly, the performance of the this mainframes depends on the computer operator or compiler as the information of the compiler plays a vital role while changing the CISC cipher to a RISC cipher
- While rearranging the process, labeled as a code extension, will growth the size. And, the quality of this code development will over depend on the compiler, and also on the machine's order set.

- The first level cache of this processor is also a drawback of the RISC, in which these mainframes have large memory caches on the chip itself. For breast-feeding the directions, they require very fast memory systems.

5. CONCLUSION

This processor was designed with high speed and it is achieved in low power. We can effortlessly decrease the power dissipation This design can be used for low power applications to enhance the sequence lifetime of the procedures. Power can be reduced further by smearing this technique at a higher level of granularity. Thus the design and application of a Processor using Timer technique to reduce power dissipation has been accomplished.

The benefit of the planned chip is, it can handle an interrupt quick and efficiently. It inhabits less area and consumes less power. More over a combined CPU in the design performs the required operations related to interrupt controller apart from the regular operation. The possibility for increasing the number of interrupts up to data bus width is provided in the design and also extended to multiprocessor.

REFERENCES

[1] Gated Clock Routing for Low-Power Microprocessor Design, Jaewon Oh and MassoudPedram, Senior Member, IEEE. IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 20, NO. 6, JUNE 2001

[2] LANG, T., MUSOLL, F, and CORTADELLA, J.: „Individual flip-flops with gated clocks for low power datapaths", IEEE Trans. Circuits S y ~ tI.I, 1997, 44, (6), pp. 507 516

[3] Xiaotao Chang, Mingming Zhang, Ge Zhang, Zhimni Zhang and Jim Wang,"Adaptive Clock Gating Technique for Low Power IP Core in SoC Design",IEEE International Symposiumon Circuits And Systems,May(2007),pp. 2120 – 2123, 2007.

[4] IBM, Multiprocessor Interrupt controller Data Book, March, 2006.

[5] Kamaraju.M, LalKishore.K, Tilak.A.V.N "A Novel Implementation ofApplication specific Instruction – set processor (ASIP) using verilog" Waste Issue 59,Nov 2011

[6] Jin Soo Kim Sunwoo, Myung H. Sunwoo, "Three low power ASIP processor designs for communications, video, and audio applications", International Conference on Design & Technology of Integrated Systems in Nanoscale Era, 2007. DTIS, pp. 241-244.

[7] Y. Takahashi, T. Sekine, and M. Yokoyama, VLSI implementation of a 4_4-bit multiplier in a two phase drive adiabatic dynamic CMOS logic. , IEICE Trans. Electron., vol. E90-C, no. 10, Oct. 2007, in press.

[8] Qiao Ying-xu, Design of Wireless Sensor Networks Node Based OnTinyOS Operating System.The 3th International Conference on Computer Science and Education[C] 2008.7 1201-1204.

[9] Jilin Li,"Status and Development Trend of Coal M i n e Safety Monitoring System", Journal, Coal Technology, Harbin, 2008(l1), pp. 4- 5.

[10] Wei Chipni, Li Ahaolin, ZhengQingwei,YeJianfei, and Li Shenglong, "Design of a configurable multichannel interrupt controller", Second Pacific-Asia Conference on Circuits, Communications and System, vol. 1,Aug 2010, pp. 327–330.

[11] PizhouYe,andChaodong Ling, "A RISC CPU IP core",Second International Conference on Anti-counterfeiting,Security and Identification ,August(2008), pp. 356–359,2008.

[12] H. Jacobson,P. Bose, ZhigangHu,A. Buyuktosunoglu, V.Zyuban,R. Eickemeyer,L. Eisen,J. Griswell,D. Logan,BalaramSinharoy, and J. Tendler," Stretching the limits of clock-gating efficiency in server-class processors",Eleventh International Symposium on High-performance Computer Architecture,Feburary (2005), pp . 238- 242, 2005.

[13] Xiaotao Chang, Mingming Zhang, Ge Zhang, Zhimni Zhang and Jim Wang,"Adaptive Clock Gating Technique for Low Power IP Core in SoC Design",IEEE International Symposium on Circuits And Systems,May(2007),pp. 2120 – 2123, 2007..

[14] S. Ghosh, D. Mohapatra, G. Karakonstantis and K. Roy," Voltage Scalable High-speed Robust Hybrid Arithmetic Units Using Adaptive Clocking"IEEE Transactions on Very Large Scale Integration Systems,September(2010),Vol. 18, pp.1301- 1309,2010.

[15] Hai Li, S. Bhunia,Y. Chen,T.N. Vijaykumar and K.Roy," Deterministic clock gating for microprocessor power reduction", Ninth International Symposium on High-Performance Computer Architecture, February (2003), pp. 113 – 122, 2003